ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT AND METHOD OF OPERATION

Abstract of the Disclosure

An ESD protection circuit (201) is for use with a high-voltage tolerant I/O circuit in an IC. This is accomplished by providing a small ESD diode (217) from the I/O pad to a relatively small boosted voltage bus (BOOST BUS). The BOOST BUS is used to power a trigger circuit (203). This path has very little current flow during an ESD event due to minimal current dissipation in the trigger circuit. There is a diode drop but only very little IR voltage drop from the I/O pad to the trigger circuit (203). The trigger circuit (203) controls relatively large cascoded clamp NMOSFETs (207, 209). The net result is that a gate-to-source voltage (VGS) of both of the clamp NMOSFETs is increased thus increasing the conductivity of the cascoded clamp NMOSFETs (207, 209). This reduces the on-resistance of each of the NMOSFETS (207, 209), thereby improving the ESD performance, and reducing the layout area required to implement robust ESD protection circuits.